(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 504 411 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
17.06.1998 Bulletin 1998/25

(21) Application number: **91916592.8**

(22) Date of filing: **19.09.1991**

(51) Int Cl.[6]: **H01L 23/04**, H01L 23/50, H01L 23/12

(86) International application number:
PCT/JP91/01242

(87) International publication number:
WO 92/05583 (02.04.1992 Gazette 1992/08)

(54) **SEMICONDUCTOR DEVICE HAVING MANY LEAD PINS**

HALBLEITERVORRICHTUNG MIT EINER VIELZAHL VON ANSCHLUSSSTIFTEN

DISPOSITIF A SEMI-CONDUCTEUR COMPORTANT DE NOMBREUSES BROCHES A FILS CONDUCTEURS

(84) Designated Contracting States:
DE GB

(30) Priority: **19.09.1990 JP 249348/90**
19.09.1990 JP 249349/90

(43) Date of publication of application:
23.09.1992 Bulletin 1992/39

(73) Proprietor: **FUJITSU LIMITED**
Kawasaki-shi, Kanagawa 211 (JP)

(72) Inventor: **TANIZAWA, Tetsu, Fujitsu Limited**
Kanagawa 211 (JP)

(74) Representative:
Schmidt-Evers, Jürgen, Dipl.-Ing. et al
Patentanwälte
Mitscherlich & Partner,
Postfach 33 06 09
80066 München (DE)

(56) References cited:
FR-A- 2 622 741
JP-A- 1 230 264
JP-A- 1 318 251
JP-A- 2 030 172
JP-A- 2 106 943
JP-A- 2 125 650
JP-A- 2 148 860

- **PATENT ABSTRACTS OF JAPAN vol. 12, no. 60 (E-584)23 February 1988**

EP 0 504 411 B1

Printed by Jouve, 75001 PARIS (FR)

Description

FILED OF THE INVENTION

The present invention relates to a semiconductor device, and particularly to a semiconductor device with a high lead density in the package.

BACKGROUND ART

FIGs. 1A and 1B are cross-sectional views of an example semiconductor device belonging to the prior art.

FIG. 1A is a cross-sectional view of a semiconductor device comprising a high-power chip and a heat sink. Bumps are formed on the face of the chip with the elements, and are bonded to TAB (Tape Automated Bonding) leads 12. This assembly is mounted onto and connected with a layer-built ceramic package. A large number of regularly spaced surface mount pins 14 project perpendicularly from an underside of this ceramic package. Power is supplied, and signals are input and output through these pins 14.

The chip 11 is encased in a metal cap 15 with its top side partially exposed. A heat sink 27 is soldered or brazed onto a top side of the chip 11, through a metal plate 16. The metal plate 16 is made of a material such as CuMo, in an attempt to make compatible the coefficients of thermal expansion of the chip 11 and of the aluminum heat sink 17.

FIG. 1B is a partial cross-sectional view of the package shown in FIG. 1A. The ceramic package 13 is constructed of ceramic layers on which is formed a pattern 13a or a power plane 13b. The pattern 13a and the power plane 13b are connected to corresponding pins 14 in the same process that the chip 11 is connected to the TAB leads 12 on which the chip is mounted by means of the bump.

The semiconductor device illustrated in FIGs. 1A and 1B is of a PGA (Pin Grid Array) type designed for increased pin population and high pin density, allowing a plurality of leads 13 to project from the underside of the package 13.

When surface mounting the semiconductor device onto the board, it is necessary to visually confirm whether has been successfully connected to the board. Since visual inspection is performed by microscope and other means, the pins 14 are provided at a periphery of the underside of the ceramic package 13, within the range where visual inspection is possible, as shown in FIGs 1A and 1B.

There is a disadvantage in this, in that visual inspection is limited to 4-6 rows of pins, prohibiting pin array placement toward the center region, and creating an area that is not usable.

From JP-A-2-125650 a semiconductor device is known having lead pins on th und rside of its package and respective pairs of ground and V_{cc} pins provided within the innermost ones of said lead pins.

The package for a semiconductor IC known from JP-A-2-30172 has, in addition to lead pins attached to the bottom of the package body, pins attached to the four sides in a horizontal direction of the package body as in a flat package.

The LSI package known from JP-A-1-230264 has, in addition to lead pins for mounting on the surface of a circuit board, additional pins provided at the four carriers of the package which are longer for mounting in through holes of the circuit board and have a larger cross-sectional area for improving the bonding strength.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a semiconductor device capable of eliminating the aforementioned disadvantage.

A more specific object of the present invention is to provide a semiconductor device that allows pins to be provided on the entire underside of a package, without having to leave any area thereof unused, and that eliminates the necessity of visual inspection.

The objects of the present invention can be achieved by a semiconductor device as set out in claim 1, comprising a predetermined number of surface mount lead pins provided at the periphery of the underside of a package fitted with a chip; and at least one lead part each lead part provided being assigned for a specific use, and being provided near the center region of the underside of the package, beyond the region populated with lead pins.

An alternative embodiment of the invention is set out in claim 2.

The objects of the resent invention can also be achieved by a semiconductor device as set out in claim 3 comprising a predetermined number of surface mount lead pins provided at the periphery of the underside of a package fitted with a predetermined number of chips; thin films built with interposed layers of film etched with desired patterns, for connecting the chips and the lead pins; and lead parts each assigned for a specific use and being thicker than the lead pins, provided near the center region of the underside of the package beyond the periphery populated with the lead pins, and optionally connected directly to the chips.

In a preferred embodiment a predetermined number of lead terminals project from all four sides of the package.

BRIEF DESCRIPTION OF THE DRAWINGS

A more clear understanding of other objects, characteristics and utility of the present invention will be obtained by reading the explanation given below with reference to the drawings detailed below.

FIGs. 1A and 1B are cross-sectional views of an embodiment of a semiconductor device of the prior art.

FIG. 2 illustrates a first embodiment of the present

invention.

FIGs. 3A to 3F illustrate a fabrication process of the embodiment of FIG. 2.

FIG. 4 illustrates a second embodiment of the present invention.

FIG. 5 illustrates a third embodiment of the present invention.

FIG. 6 illustrates a variation of the embodiment of FIG. 5.

FIGs. 7A, 7B, 8A, 8B, 9A and 9B illustrate variations of any of the first, second or third embodiments above.

FIG. 10 illustrates a fourth embodiment of the present invention.

FIGs. 11A to 11C illustrate a variant of the present invention.

FIGs. 12A to 12D illustrate an example fabrication process of the variant of FIGs. 11A to 11C.

FIGs. 13A to 13I illustrate an example fabrication process of a thin film such as the one shown in FIG. 12A.

FIGs. 14A and 14B illustrate another example fabrication process of the embodiment of FIGs. 11A to FIG. 11C.

FIG. 15 illustrates a further variant of the present invention.

FIGs. 16A and 16B illustrates a further variant of the present invention.

FIGs. 17A and 17B illustrate a fifth embodiment of the present invention.

BEST MODE OF CARRYING OUT THE INVENTION

FIG. 2 illustrates a first embodiment of the present invention. The semiconductor 11 of FIG. 2 is, for example, a high-power chip and is provided with a heat sink 17, a metal cap 15, and a metal plate 16 between the heat sink and the metal cap. Bumps are formed on the face of the chip 11 with the elements, and are bonded to TAB leads 12. Bumps can alternatively be formed on the TAB leads 12. The assembly is mounted onto and connected with a ceramic package 13.

Regularly spaced lead pins 14 (for signals for example), are provided projecting perpendicularly from the underside of the package, in 5 rows for example, at the periphery of the ceramic package. These lead pins 14 are surface mount lead pins, and are connected to the pattern formed in respective layers within the multi-layer ceramic package 13 (see FIG. 1B).

Cylindrical lead pins 22, are provided, as lead parts each assigned for a specific use, toward the interior 21 of the underside of the ceramic package 13, beyond the region populated with the lead pins 14, in 4 groups of 9 pins each, for example (see FIG. 4). Cylindrical lead pins 22 each assigned for a specific use include, for example, power lead pins 22a and 22c or ground lead pins 22b and 22d. They are larger than the lead pins 14 in thickness, and are formed for surface mount. Their use makes power circuit connection easy.

The lead pins 22 need not be cylindrical in shape, but can be of any shape including octagonal columns or hexagonal columns. The lead pins 22 are made of the same material as the lead pins 14 and are plated with gold, for example. The reason for forming the lead pins 22 thicker than the lead pins 14 is to ensure, in the present invention, that electric connection is established by eliminating a slight displacement that occurs in prior art when mounting a semiconductor device onto the board. Accordingly, the lead pins 22 are more sparsely spaced than the lead pins 14.

While in the above embodiment a plurality of lead pins 22 are provided, providing at least one lead pin 22 ensures performance.

When a semiconductor device as the one described in the above embodiment is mounted onto a board, electric connection of 5 rows of lead pins 14 with the board is confirmable visually. The necessity of visual inspection of the lead pins 22 provided in the interior 21 is eliminated since the connection of one pin alone among 9 ensures performance.

This way, it is possible to avoid leaving any unused room on the entire underside of the ceramic package 13, in providing pins. It also becomes possible to assign the lead pins 14, provided in the periphery, for signal use only, thus allowing provision of a denser array useful for decreasing capacitance and resistance, improving high-frequency properties, and increasing the chance of down-scaling the entire composite.

FIGs. 3A to 3F illustrate an example fabrication process of the embodiment of FIG. 2. First, a TAB film 32 is prepared on which TAB leads 12 are formed corresponding to a plurality of pads 31 placed on the chip 1 (FIGs. 3A, and 3B). Bumps are formed either on the pads 31 of the chip 11 or on an end of each TAB lead 12, or on both. The chip 11 is joined with the TAB leads 12 by bonding. Then the TAB leads 12 are cut from the TAB film 32 (FIG. 3C).

The ceramic package 13 is formed by building layers of ceramic on which specific patterns 33 have been formed. The lead pins 14 and the lead pins 22 project from the underside of the package as shown in FIG. 2 (FIG. 3D). The edge of the pattern on the uppermost layer in the ceramic package and the edge of the TAB leads 12 joined with the chip 11 are bonded by means of face down bonding (FIG. 3D).

A metal cap 15 is then soldered or brazed above the uppermost layer of the ceramic package 13 in such a way as to encase the chip 11 (FIG. 3E). A metal plate 16 is soldered or brazed onto this metal cap 15 and the chip 11, then a heat sink 17 is soldered or brazed onto the metal plate 16 (FIG. 3F). The metal cap 15, the metal plate 16 and the heat sink 17 may be joined together in advance.

FIG. 4 illustrates a second embodiment of the present invention. A semiconductor device in FIG. 4 is shown mounted on a board 42. The semiconductor herein is essentially the sam as in FIG. 2 except that it is provided with lead pins 41 (power pins 41a and

ground pins 41b, specifically) obtained by extending the lead pins 22 of the previous embodiment so that they are longer than the lead pins 14 at the periphery. In this case, corresponding positions on the board for mounting of the composite, are provided with through-holes 44a to allow the lead pins 41 to go through. In other words, the lead pins 14 at the periphery are surface mounted, while the lead pins 41 are mounted by soldering, for example by allowing them to go through the through-holes 42a.

The above construction allows the lead pins 41 to serve as an insertion guide into the through-holes 42a, facilitating alignment during surface mount. Direct connection of the lead pins 41 with the board 42 decreases the inductance component.

Connection of the lead pins 41 with the board 42 can easily be inspected visually by looking at underside of the board 42 since the lead pins 41 go through the board 42.

FIG. 5 is a bottom view of a third embodiment of the present invention. In a semiconductor device shown in FIG. 5, the lead pins 22 (41) such as those shown in FIGs.2 and 4 are provided in such a manner that they encompass terminal(s) 51 assigned for use as, for example, clock pins in semiconductor circuits. It is possible thus to attain increased stability in the operation of the device due to encompassing the terminal(s) 51 with the lead pins 22 (41), which are not susceptible to fluctuation in potential as they are assigned as power and signal pins, thus preventing noise.

The terminal(s) 51 can ensure a secure mounting, by eliminating displacement that occurs when mounting the composite on the board, by forming the terminal(s) so as to be thicker than the lead pins 14 as in the case of the lead pins 22 (41).

FIG. 6 illustrates a variation of the embodiment of FIG. 5. The terminal(s) 51 in FIG. 6 are formed longer than the lead pins 22. In this case, through-holes 42a are drilled on a board 42 for mounting of the composite, and the terminals 51 come through the through-holes 42a to be soldered on the board. Here, the terminals 51 can serve as a guide in mounting. Alternatively, the lead pins here can be like the lead pins 41 in FIG. 4, which are longer than the lead pins 14. They can also go through the board 42 and be fixed. By using these methods, visual inspection of the solder joint is possible from the underside of the board.

FIGs. 7 to 9 illustrate variations of the above embodiment.

FIG. 7A is a cross-sectional view, and FIG. 7B is a partial bottom view. (Note that the chip 11 on upper side, the heat sink 17, etc. will be left out of the diagrams hereinafter through FIG. 9B). The semiconductor device in FIGs. 7A and 7B is fabricated in such a way that square-shaped one or more lead parts 71 that look like a block are provided toward the interior 21 on the underside of the packag 13 beyond the r gion populated with the lead pins 41. These lead parts 71 can be assigned as power pins in the semiconductor circuit, for example. With this semiconductor it is possible to achieve a wide contact area with the board when mounting the composite, and to have the composite soldered to the corresponding pattern on th board with accuracy, even when displacement occurs. This way, the process of visual inspection of connections can be eliminated.

FIG. 8A is a partial cross-sectional view, and FIG. 8B is a partial bottom view. The semiconductor device shown in FIGs. 8A and 8B is fabricated in such a way that cylindrical block-shaped lead parts 81 are provided in place of the lead parts 71 shown in FIGs. 7A and 7B, for the same use. These lead parts 81 are spaced more sparsely than the lead pins 14 and are surface mounted as in FIGs. 7A and 7B. Accordingly, because the lead parts 81 are block-shaped, a more secure connection with the board is achieved, and the process of visual inspection can be eliminated.

FIG. 9A is a partial cross-sectional view, and FIG. 9B is a partial bottom view. The semiconductor device shown in FIGs. 9 and 9B is fabricated in such a way that lead parts having L-plate shape, are provided in place of the lead parts 71 or 81 above. The usefulness of this configuration when the composite is mounted on the board is the same as that of the configuration with the lead parts 71 or 81.

FIG. 10 illustrates a fourth embodiment of the present invention. The semiconductor device shown in FIG. 10 is fabricated in such a way that a high-power chip 111 is mounted on a depression 113a formed on a metal base 113a. A thin film 112 is positioned on the same plane as the upper surface of the chip. The chip is joined to the thin film 112 on both ends of the face with the elements, through TAB leads 114, with the use of bumps. These thin films 112a and 112b are TABs produced by layering thin films (made of polyimide, etc.) etched with fine patterns, and are supplied with signal pads (described later) for connection with the TAB leads 114 and pins to be described later. That is, this thin film 112 acts to disperse the layout of the lead pins connected thereto. The metal base 113 on which the chip 111 and other things are mounted is soldered or brazed to an underside of a heat sink 115 formed of a material such as aluminum. This metal base 113 is formed of a material such as CuMo, and is designed for making compatible the coefficients of thermal expansion between the chip 111 and the heat sink 115 as they are bonded together.

The package 116 is fabricated in such a way that it allows signal lead pins 14 to project at the periphery of its underside; it also allows lead pins 22, each assigned for a specific use, to project from a region toward the interior 21 of the underside, and is provided with a depression (PGA type). The signal lead pins 14 project perpendicularly in 4 to 6 rows and are spaced regularly, so that they can be visually inspected when mounted on th board. The package 116 comprises layers of ceramic etched with a power plane 117, which is a power sup-

ply pattern. A predetermined number of lead pins 22 connected with the power plan 117 is provided in the interior 21 on th underside of the package 116. These lead pins 22 are formed thick enough to make them differentiable from the signal lead pins 14, and to eliminate displacement while mounting the composite onto the board. They are used, for example, as power pins, or as clock pins sealed by the power pins.

The package 116 is then fitted to the metal base 113 with adhesive, for example. The signal lead pins 14 are electrically connected with signal pads on the thin film 112 through contact pins 118a placed in a pressurized contact with the pins. Some of the lead pins 22 and power supply pads formed on the chip 111 are electrically connected through contact pins 118b.

A semiconductor device such as this can be made thin since it requires only the power plane 117 inside the package 116. Use compatible with semiconductor devices having chips of other functions is also possible. Direct contact of the power lead pins 22 with the chip 2 assures low impedance because an intermediate conductor pattern is eliminated. Moreover, even if the metal base 113 is taken away from the package 116 it is restorable since the connections among the lead pins 14, the lead pins 22, the chip 111, and the thin film 112 are achieved by pressurized contact only, with the use of the contact pins 118a and 118b. This makes failure analysis of the device easier, and improves fabrication yield. Moreover, since a group of inner power leads 12 are provided in the interior 14, thus increasing the likelihood that electric contact is established, the process of visual inspection of the connection can be eliminated when mounting such a semiconductor device onto the board.

While FIG. 10 shows the electric connection of the lead pins 14 and 22 with the thin film 112 achieved by means of the contact pins 118a and 118b, use of bumps instead can make the device smaller in proportion to the dimensions of the contact pins 118a and 118b.

Direct connection of some of the lead pins 12 with the chip 111 in this embodiment may be replaced by another connection means, wherein the pins are connected with the chip 111 through the thin film 112 by means such as TAB leads, for example. In this manner the structure is simplified and crosstalk arising from the signal lead pins 14 is prevented.

The lead pins 22 can also serve as a guide when mounting the composite if they are made longer than the lead pins 14, as shown in FIG. 4.

FIGs. 11A to 11C illustrate a variant of the fourth embodiment of the present invention. In this variant, the contact pins 118a and 118b in FIG. 10, used for connections among the lead pins 14, 22, the film 112 and the chip 111, are replaced by bumps. Accordingly, FIGs. 11A to 11C are partial cross-sectional views showing an area in which bumps are formed. Configuration other than as concerns th bumps remains the same as in FIG. 10.

FIG. 11A is a part of a top cross-sectional view, and FIG. 11B is a part of its side cross-sectional view showing a relationship betwe n a chip and a thin film. In FIGs. 11A and 11B, a chip 111 is mounted onto a metal base 113. In the periphery of the chip, the thin film is positioned on the same plane as the topside of the chip. A signal pattern 119a, for example, and a power pattern 119b, for example, are formed on the thin film 112, each layer being connected by through-holes.

The topmost pattern 119a of the thin film 12 is bumped (120) at one end thereof, while the other end is connected to a pad 121 of the chip 111 via a TAB lead 114. Around the thin film 112 is formed a seal pattern 122. The thin film 112 here differs from the thin film 112 in FIG. 10 in that it comprises a bump.

FIG. 11C illustrates a relationship between the thin film and the lead pins. FIG. 11C shows that the bump 120 formed on the pattern 119a of FIGs. 11A and 11B, and the bump 120 formed on the pattern 122 provided on the surface of the package 116 are completely joined by pressure. This happens between each pattern 119a and a corresponding lead pin 14, so as to establish an electrical connection.

FIGs. 12A to 12D illustrate an example fabrication of the device of FIGs. 11A to 11C. First, FIG. 12A shows that a thin film 112 having an opening 112a that corresponds to a depression 113a is formed around the depression 113a provided in a metal base 113 attached to a heat sink 15. FIG. 12B shows a chip 111 mounted onto the depression 113a of the metal base 113. FIG. 12C shows that the chip 111 and the thin film 112 are connected via TAB leads 114, as shown in FIGs. 11A and 11B. Bumps 120 are formed on the interface between the chip 111 and the thin film 112. FIG. 12D shows that the patterned portion of a package 116 formed so as to connect to lead pins 14 and 22 projecting from the surface of the package 116, is bumped (120). Connection is established by pressure joining the bumps 120 against the corresponding bumps 120 formed on the chip 111 and the thin film 112 so that the connection is complete. The package 116 and the periphery of the metal base 113 are then sealed by soldering.

The semiconductor device of the prior art shown in the FIG. 1 has a disadvantage in that it is difficult to judge whether such parts as the chip and the metal base are firmly united. It also leaves a possibility of solder leakage between the chip and the metal base. With the semiconductors fabricated in the process of the present invention, on the other hand, it is sufficient to have the periphery of the package 116 and the metal base 113 united; inspection is easy.

The power lead pins 22 can be alternatively connected via the thin film 112 by providing a pattern on the package 116, thus eliminating a direct connection with the chip 111. In this way crosstalk can be avoided just as surely as in the above mentioned manner.

FIGs. 13A to 13I illustrate an example process for forming the thin film such as the one shown in the FIG. 12A. First, a metal layer 131 is formed on a metal base (FIG. 13A) by a method such as evaporation (FIG. 13B).

The metal layer 131 is treated with photoresist 132 (FIG. 13C), and a pattern 132a is formed after lithography and a development process (FIG. 13D). The metal layer 131 is then etched to create a pattern 131a (FIG. 13E). The photoresist pattern 132a is then removed (FIG. 13F).

Photosensitive polyimide 133 is then spin coated onto the metal pattern 131a (FIG. 13G), which is exposed after the lithography and development process. After the polyimide 133 is hardened by heating (FIG. 13H), metal layer 134 is formed by a process such as evaporation, and is connected with the metal pattern 131a below (FIG. 13I).

A repetition of these processes in building 4 or 5 layers forms a thin film 112.

Although it is not shown in the figure, an opening 112a of FIG. 12A is formed in each layer formed in the above process.

FIGs. 14A and 14B illustrate another example fabrication process of device of FIGs. 11A to 11C. FIG. 14A shows a process in which the opening 112a of the FIG. 12A is not formed, but wherein a thin film 112 is formed by building 4 or 5 layers of patterned polyimide on a metal base 113 (see FIGs. 13A to 13I). A chip 111 is mounted onto this thin film 112, and the chip 111 and the pattern on the thin film 112 are bonded by a wire 141. Bumps 120 are formed on one end of a pattern 119a on the thin film 112 and on a pad 121 on the chip 111.

FIG. 14B shows a pattern 142 formed on a layer-built package 116 comprising lead pins 14 and 22 projecting from the underside of the package. Bumps 120 are formed on the end of the pattern. Pressure joining the bumps 120 on the chip 111 and the thin film 112 to the corresponding bumps 120 on the pattern 142 unites the composites.

FIG. 15 illustrates a further variant of the fourth embodiment of the present invention. A semiconductor device shown in FIG. 15 is a side cross-sectional view of a multi-chip embodiment. FIG. 15 shows chips 111 and 111A connected through TAB leads 114A. Other configurations remain the same as the semiconductor device of FIG. 10. This exemplifies a multi-chip embodiment, which was impossible in the prior art.

While FIG. 15 shows the chips 111 and 111A connected through the TAB leads 114A, this arrangement can be replaced by a configuration where a thin film comprising patterned polyimide layers is interposed between the chips 111 and 111A so that TAB leads can connect them.

Connection between the chips 111 and 111A, and the thin film 112 can be accomplished by wire-bonding as illustrated in FIG. 14 and 14B.

In the two variants of the fourth embodiment above, the lead pins 22 are described as having the role, in surface mounting, as in the embodiment of FIG. 2. Accordingly, the function of these lead pins 22 is the same as that described in FIG. 2. When extended to be as those shown in FIG. 4, these lead pins function in th same way as in the embodiment of FIG. 4. When terminal(s) 51 are provided as shown in FIGs. 5 and 6, the terminals have the same function as in FIGs. 5 and 6. The lead pins 22 may alternatively be formed into shapes as shown in any of FIGs 7 to 9.

While the use of ceramic package was assumed in th first to fourth embodiments above, a package formed with such resin as epoxy, or metal, also assures performance. Further, these embodiments have the same utility with semiconductor devices fitted with a chip not needing a heat sink.

FIGs. 16A and 16B illustrate an embodiment of a semiconductor device. While the use of a PGA type semiconductor device was assumed in any of the first to fourth embodiments above, this embodiment comprises a QFP (Quad Flat Package) type semiconductor device.

In the semiconductor device shown in FIGs. 16A and 16B, lead pins 162 project from all four sides of a package (ceramic or resin mold) 161, and are shaped like an L-plates for the purpose of surface mount. Moreover, at least one lead part 163 project from the underside of the package. Provided lead part 163 can be of any form including those of the lead pins 22, 41, and the lead parts 71, 81, 91 above. Clock terminal(s) 51 are provided, when needed. With this configuration, the vacant region of a QFP type package can be utilized effectively.

FIGs 17A and 17B illustrate a variation of the embodiments of FIG. 16 as a fifth embodiment of the present invention. In a QFP type semiconductor shown in FIG. 17, lead part(s) 171 with the shape of an L-plates are provided on the underside of a package 161.

Thus, any of the first to fifth embodiments show that it is possible to provide pins effectively by providing lead parts, each assigned for specific use, in the otherwise unoccupied region on the underside of the package, and to ensure the connection is established when mounting the composite onto the board, and to eliminate the process of visual inspection. The present invention also makes layer-building of the package easy and facilitates down-scaling. Providing power lead parts on the underside of the package ensures a high density of signal lead pins, and increases the capacity of a semiconductor integrated circuit.

POSSIBLE APPLICATION IN INDUSTRY

As explained above, the present invention allows effective pin array placement on the entire underside of a package, and eliminates the process of visual inspection when mounting the composite onto the board, thus realizing high density and greater capacity of the semiconductor device.

The present invention can find applications in high-density semiconductor devices including a PGA type and a QFP type.

Claims

1. A semiconductor device, comprising

a predetermined number of first lead pins (14) provided on an underside of a package (13), fitted with a chip (11), at a periphery of said underside; and
a plurality of second lead pins (22), each having a specific circuit function, provided on said underside of said package (13) at an interior region of said underside beyond that periphery region at which said first lead pins (14) are provided, wherein at least two lead pins (22) of said second lead pins have a same circuit function and said same circuit function is fulfilled by connecting anyone of said at least two lead pins (22) to conductive members on a circuit board on which said device is to be mounted,
said first and second lead pins (14, 22) having end portions connectable to a surface of said circuit board,

characterized in that

said first and second lead pins (14, 22) are provided on said underside of said package (13) so that substantially no area of said underside has to be left unused;
said second lead pins (22) are provided in a plurality of groups, each of said groups having a specific circuit function and the pins of each group having the same specific circuit function; and
the distance between adjacent groups is greater than the distance between the lead pins in anyone of said plurality of groups.

2. A semiconductor device, comprising

a predetermined number of first lead pins (14) provided on an underside of a package (13), fitted with a chip (11), at a periphery of said underside; and
at least one second lead pin (41), each having a specific circuit function, provided on said underside of said package (13) at an interior region of said underside beyond that periphery region at which said first lead pins (14) are provided,
said first lead pins (14) and said at least one second lead pin (41) having end portions connectable to a surface of a circuit board,

characterized in that
said at least one second lead pin (41) is longer than said first lead pins.

3. A semiconductor device, comprising

a predetermined number of first lead pins (14) provided on an underside of a package (16) at a periphery of said underside, wherein said package is fitted with a plurality of different types of chips (111, 111A) and said chips (111, 111A) are mounted on said package (16);
at least one second lead pin (22, 41), each having a specific circuit function and being formed thicker than said first lead pins (14), connected to said chips (111) and provided on said underside of said package (16) at an interior region of said underside beyond that periphery region at which said first lead pins (14) are provided; and
multilayer thin films (112) being etched with desired wiring patterns and interposed between said chips (111, 111A) and said first lead pins (14) for connecting said chips (111, 111A) and said first lead pins (14), said multilayer thin films (112) being mounted on said package (16);
wherein said at least one second lead pin (22, 41) is connected to said chips (111, 111A) without the interposition of said wiring patterns on said multilayer thin films (112).

4. A semiconductor device according to claim 3, **modified in that**
also said at least one second lead pin (22, 41) is connected to said chips (111, 111A) through the interposition of said multilayer thin films (112).

5. A semiconductor device according to claim 3 or 4, **characterized in that**
a connection between said chips (111, 111A) is accomplished through the interposition of said multilayer thin films (112).

6. A semiconductor device according to claim 1 or 2, **characterized in that**
said first lead pins (162) extend beyond the sides of said package (161).

7. A semiconductor device according to anyone of claims 1 to 6, **characterized in that**
said second lead pins or said second lead pin (22, 41, 163) serve or serves as a power supply system for said chip (111) or said chips (111, 111A).

8. A semiconductor device according to claim 1 or 2, **characterized in that**
said second lead pins (22, 41, 163) are thicker than said first lead pins (14).

9. A semiconductor device according to claim 1, **modified in that**

each group of said second l ad pins (22, 41, 163) is replaced by a block-shaped lead part (71, 81).

10. A semiconductor device according to claim 1, or claim 6 when dependent on claim 1,
m difled in that
each group of said second lead pins (22, 41, 163) is replaced by an L-plate (91, 171).

11. A semiconductor device according to anyone of claims 1 to 8,
characterized by
third lead pins (51), each having a further specific circuit function and being encompassed by said second lead pins (22, 41, 163).

12. A semiconductor device according to claim 11,
characterized in that
said third lead pins (51) are longer than said first lead pins (14) so as to go through said board (42) and to be fixed onto it when mounting said device onto said board.

13. A semiconductor device according to claim 12,
characterized in that
said third lead pins (51) serve as a guide when mounting said device onto said board (42).

14. A semicondcutor device according to anyone of claims 11 to 13,
characterized in that
said third lead pins (51) serve as clock terminals in a semiconductor circuit.

Patentansprüche

1. Halbleitervorrichtung, umfassend:

eine bestimmte Anzahl von ersten Anschlußstiften (14), welche auf einer Unterseite eines Gehäuses (13), auf dem ein Chip (11) aufgesetzt ist, an einem peripheren Bereich der Unterseite vorgesehen sind, und
eine Vielzahl von zweiten Anschlußstiften (22), die jeweils eine bestimmte Schaltungsfunktion besitzen und auf der Unterseite des Gehäuses (13) an einem inneren Bereich der Unterseite jenseits des peripheren Bereichs, wo die ersten Anschlußstifte (14) vorgesehen sind, angeordnet sind, wobei mindestens zwei Anschlußstifte (22) der zweiten Anschlußstifte eine gleiche Schaltungsfunktion besitzen und die gleiche Schaltungsfunktion durch Anschließen eines beliebigen der mindestens zwei Anschlußstifte (22) an leitende Teile auf einer Leiterplatte, an der die Vorrichtung anzubringen ist, erfüllt wird, wobei die ersten und zweiten Anschlußstifte (14, 22) Endabschnitte aufweisen, die an eine Ob rfläche der Leiterplatte anschli ßbar sind,

dadurch g kennz ichn t,

daß die ersten und zw iten Anschlußstifte (14, 22) auf der Unterseite des Gehäuses (13) derart angeordnet sind, daß im wesentlichen kein Bereich der Unterseite ungenutzt ist,
daß die zweiten Anschlußstifte (22) in einer Vielzahl von Gruppen vorhanden sind, wobei jede dieser Gruppen eine bestimmte Schaltungsfunktion besitzt und die Stifte jeder Gruppe dieselbe bestimmte Schaltungsfunktion besitzen, und
daß die Entfernung zwischen benachbarten Gruppen größer als die Entfernung zwischen den Anschlußstiften innerhalb jeder der Vielzahl von Gruppen ist.

2. Halbleitervorrichtung, umfassend:

eine bestimmte Anzahl von ersten Anschlußstiften (14), welche auf einer Unterseite eines Gehäuses (13), auf dem ein Chip (11) aufgesetzt ist, an einem peripheren Bereich der Unterseite vorgesehen sind, und
mindestens einen zweiten Anschlußstift (41), der eine bestimmte Schaltungsfunktion besitzt und auf der Unterseite des Gehäuses (13) an einem inneren Bereich der Unterseite jenseits des peripheren Bereichs, wo die ersten Anschlußstifte (14) vorgesehen sind, angeordnet sind,
wobei die ersten Anschlußstifte (14) und der mindestens eine zweite Anschlußstift (41) Endabschnitte aufweisen, die an eine Oberfläche der Leiterplatte anschließbar sind,

dadurch gekennzeichnet,
daß der mindestens eine zweite Anschlußstift (41) länger als die ersten Anschlußstifte ost.

3. Halbleitervorrichtung, umfassend:

eine bestimmte Anzahl von ersten Anschlußstiften (14), welche auf einer Unterseite eines Gehäuses (16) vorhanden sind, wobei auf das Gehäuse eine Vielzahl von unterschiedlichen Arten von Chips (111, 111A) aufgesetzt und die Chips (111, 111A) an dem Gehäuse (16) befestigt sind,
mindestens ein zweiter Anschlußstift (22, 41), der eine bestimmte Schaltungsfunktion besitzt und dicker als die ersten Anschlußstifte (14) ist,
wobei der mindestens eine zweite Anschlußstift mit den Chips (111) verbunden und an d r Unterseit des Gehäuses (16) an

einem inneren Bereich der Unterseite jenseits des peripheren Bereichs, wo die ersten Anschlußstifte (14) vorgesehen sind, angeordnet ist, und
mehrlagige Dünnschichten (112), die gemäß gewünschter Verdrahtungsmuster geätzt und zwischen den Chips (111, 111A) und den ersten Anschlußstiften (14) angeordnet sind, um die Chips (111, 111A) mit den ersten Anschlußstiften (14) zu verbinden, wobei die mehrlagigen Dünnschichten (112) an dem Gehäuse (16) angebracht sind,
wobei der mindestens eine zweite Anschlußstift (22, 41) mit den Chips (111, 111A) ohne Zwischenschaltung der auf den mehrlagigen Dünnschichten (112) vorhandenen Verdrahtungsmuster verbunden ist.

4. Halbleitervorrichtung nach Anspruch 3, **dadurch modifiziert,** daß auch der mindestens eine zweite Anschlußstift (22, 41) über die dazwischen angeordneten mehrlagigen Dünnschichten (112) mit den Chips (111, 111A) verbunden ist.

5. Halbleitervorrichtung nach Anspruch 3 oder 4, **dadurch gekennzeichnet,** daß eine Verbindeung zwischen den Chips (111, 11A) über die Zwischenschaltung der mehrlagigen Dünnschichten (112) erzielt wird.

6. Halbleitervorrichtung nach Anspruch 1 oder 2, **dadurch gekennzeichnet,** daß sich die ersten Anschlußstifte (162) über die Seiten des Gehäuses (161) hinaus erstrecken.

7. Halbleitervorrichtung nach einem der Ansprüche 1 bis 6, **dadurch gekennzeichnet,** daß die zweiten Anschlußstifte bzw. der zweite Anschlußstif (22, 41, 163) als Energieversorgungssystem für die Chips (111, 111A) bzw. den Chip (111) dienen bzw. dient.

8. Halbleitervorrichtung nach Anspruch 1 oder 2, **dadurch gekennzeichnet,** daß die zweiten Anschlußstifte (22, 41, 163) dicker als die ersten Anschlußstifte (14) sind.

9. Halbleitervorrichtung nach Anspruch 1, **dadurch gekennzeichnet,** daß jede Gruppe der zweiten Anschlußstifte (22, 41, 163) durch ein blockförmiges Anschlußteil (71, 81) ersetzt ist.

10. Halbleitervorrichtung nach Anspruch 1 oder Anspruch 6, soweit dieser abhängig von Anspruch 1 ist, **dadurch g k nnz ichn t,** daß jede Gruppe der zweiten Anschlußstifte (22, 41, 163) durch eine L-Platte (91, 171) ersetzt ist.

11. Halbleit rvorrichtung nach einem der Ansprüche 1 bis 8, **gekennzeichnet durch** dritte Anschlußstifte (51), die jeweils eine weitere bestimmte Schaltungsfunktion besitzen und von den zweiten Anschlußstiften (22, 41, 163) umgeben sind.

12. Halbleitervorrichtung nach Anspruch 11, **dadurch gekennzeichnet,** daß die dritten Anschlußstifte (51) länger als die ersten Anschlußstifte (14) sind, so daß sie durch die Platte (42) verlaufen und bei Anbringen der Vorrichtung an der Platte darauf zu befestigen sind.

13. Halbleitervorrichtung nach Anspruch 12, **dadurch gekennzeichnet,** daß die dritten Anschlußstifte (51) beim Anbringen der Vorrichtung an der Platte (42) als Führung dienen.

14. Halbleitervorrichtung nach einem der Ansprche 11 bis 13, **dadurch gekennzeichnet,** daß die dritten Anschlußstifte (51) als Taktanschlüsse in einer Halbleiterschaltung dienen.

Revendications

1. Dispositif à semiconducteur, comprenant :

un nombre prédéterminé de premières broches formant des sorties, ou broches de sortie, (14), disposées sur l'envers d'un boîtier (13), assujetti à une puce (11), à la périphérie dudit envers ; et
une pluralité de deuxièmes broches formant des sorties, ou broches de sortie, (22) ayant chacune une fonction de circuit particulière, disposées sur ledit envers dudit boîtier (13) en une région interne dudit envers se trouvant au-delà de la région de périphérie où lesdites premières broches de sortie (14) sont disposées, où au moins deux broches de sortie (22) parmi lesdites deuxièmes broches de sortie ont une même fonction de circuit et ladite même fonction de circuit est remplie par connexion de l'une quelconque desdites deux, ou plus de deux, broches de sortie (22) à des éléments conducteurs se trouvant sur une carte de circuit sur laquelle ledit dispositif doit être monté,
lesdites premières et deuxièmes broches de sortie (14, 22) ayant des parties terminales qui

peuvent être connectées à une surface de ladite carte de circuit.

caractérisé en ce que :

lesdites premières et deuxièmes broches de sortie (14, 22) sont disposées sur ledit envers dudit boîtier (13) de façon que sensiblement aucune surface dudit envers ne doive rester inutilisée ;
lesdites deuxièmes broches de sortie (22) sont disposées suivant une pluralité de groupes, chacun desdites groupes ayant une fonction de circuit particulière et les broches de chaque groupe ayant la même fonction de circuit particulière ; et
la distance entre groupes adjacents est supérieure à la distance séparant les broches de sortie qui se trouvent dans l'un quelconque des groupes de ladite pluralité de groupes.

2. Dispositif à semiconducteur, comprenant :

un nombre prédéterminé de premières broches formant des sorties, ou broches de sortie, (14), disposées sur l'envers d'un boîtier (13), assujetti à une puce (11), à la périphérie dudit envers ; et
au moins une deuxième broche formant une sortie, ou broche de sortie (41), ayant, ou ayant chacune, une fonction de circuit particulière, disposée sur ledit envers dudit boîtier (13) en une région interne dudit envers se trouvant au-delà de la région de périphérie où lesdites premières broches de sortie (14) sont disposées, lesdites premières broches de sortie (14) et ladite ou lesdites deuxièmes broches de sortie (41) ayant des parties terminales qui peuvent être connectées à une surface d'une carte de circuit,

caractérisé en ce que :
ladite ou lesdites deuxièmes broches de sortie (41) sont plus longues que lesdites premières broches de sortie.

3. Dispositif à semiconducteur, comprenant :

un nombre prédéterminé de premières broches formant des sorties, ou broches de sortie, (14), disposées sur l'envers d'un boîtier (16) à la périphérie dudit envers, où ledit boîtier est assujetti à une pluralité de puces de types différents (111, 111A) et lesdites puces (111, 111A) sont montées sur ledit boîtier (16);
au moins une deuxième broche formant une sortie, ou broche de sortie, (22, 41), ayant, ou ayant chacune, une fonction de circuit particulière et présentant une plus grande épaisseur que lesdites premières broches de sortie (14), connectée auxdites puces (111) et disposée sur ledit envers dudit boîtier (16) en une région interne dudit envers se trouvant au-delà de la région de périphérie où lesdites premières broches de sortie (14) sont disposées ; et
des pellicules minces multicouches (112), qui sont gravées suivant des motifs de câblage voulus et s'interposent entre lesdites puces (111, 111A) et lesdites premières broches de sortie (14) afin de connecter lesdites puces (111, 111A) et lesdites premières broches de sortie (14), lesdites pellicules minces multicouches (112) étant montées sur ledit boîtier (16);
où ladite ou lesdites deuxièmes broches de sortie (22,41) sont connectées auxdites puces (111, 111A) sans interposition desdits motifs de câblage sur lesdites pellicules minces multicouches (112).

4. Dispositif à semiconducteur selon la revendication 3,

modifié en ce que :
ladite ou lesdites deuxièmes broches de sortie (22, 41) sont également connectées auxdites puces (111, 111A) via l'interposition desdites pellicules minces multicouches (112).

5. Dispositif à semiconducteur selon la revendication 3 ou 4,

caractérisé en ce que :
une connexion entre lesdites puces (111, 111A) est réalisée via l'interposition desdites pellicules minces multicouches (112).

6. Dispositif à semiconducteur selon la revendication 11 ou 2,

caractérisé en ce que :
lesdites premières broches de sortie (162) s'étendent au-delà des côtés dudit boîtier (161).

7. Dispositif à semiconducteur selon l'une quelconque des revendications 11 à 6,

caractérisé en ce que :
lesdites deuxièmes broches de sortie ou ladite deuxième broche de sortie (22, 41, 163) font fonction de système d'alimentation électrique pour ladite puce (111) ou lesdites puces (111, 111A).

8. Dispositif à semiconducteur selon la revendication 1 ou 2,

caractérisé en ce que :
lesdites deuxièmes broches de sortie (22, 41, 163) sont plus épaisses que lesdites premières broches de sortie (14).

9. Dispositif à semiconducteur selon la revendication

1,

modifié en ce que :

chaque groupe desdites deuxièmes broches de sortie (22, 41, 163) est remplacé par une partie formant une sortie en forme de bloc (71, 81).

10. Dispositif à semiconducteur selon la revendication 1, ou selon la revendication 6 dépendant de la revendication 1,

modifié en ce que :

chaque groupe desdites deuxièmes broches de sortie (22, 41, 163) est remplacé par une plaque en L (91, 171).

11. Dispositif à semiconducteur selon l'une quelconque des revendications 11 à 8,

caractérisé par :

des troisièmes broches formant des sorties, ou broches de sortie. (51), ayant chacune une autre fonction de circuit particulière et étant entourée par lesdites deuxièmes broches de sortie (22, 41, 163).

12. Dispositif à semiconducteur selon la revendication 11,

caractérisé en ce que :

lesdites troisièmes broches de sortie (51) sont plus longues que lesdites premières broches de sortie (14) de façon à passer au travers de ladite carte (42) et à être fixées sur celle-ci lors du montage dudit dispositif sur ladite carte.

13. Dispositif à semiconducteur selon la revendication 12,

caractérisé en ce que :

lesdites troisièmes broches de sortie (51) font fonction de guide lors du montage dudit dispositif sur ladite carte (42).

14. Dispositif à semiconducteur selon l'une quelconque des revendications 11 à 13,

caractérisé en ce que :

lesdites troisièmes broches de sortie (51) font fonction de bornes d'horloge dans un circuit à semiconducteur.

FIG. 1A

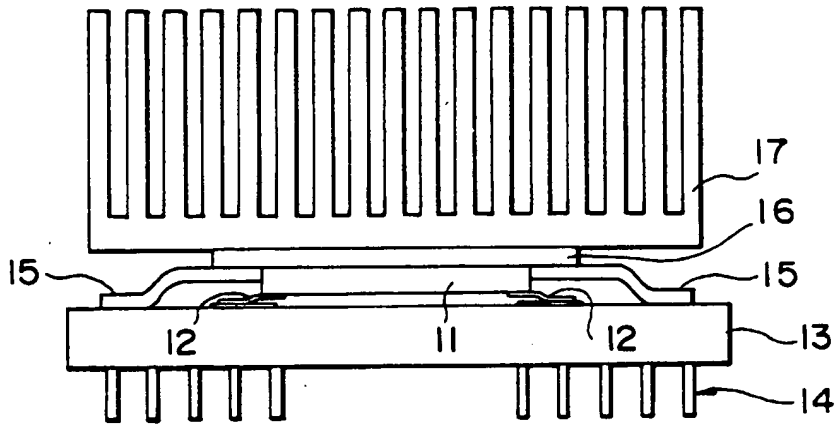

FIG. 1B

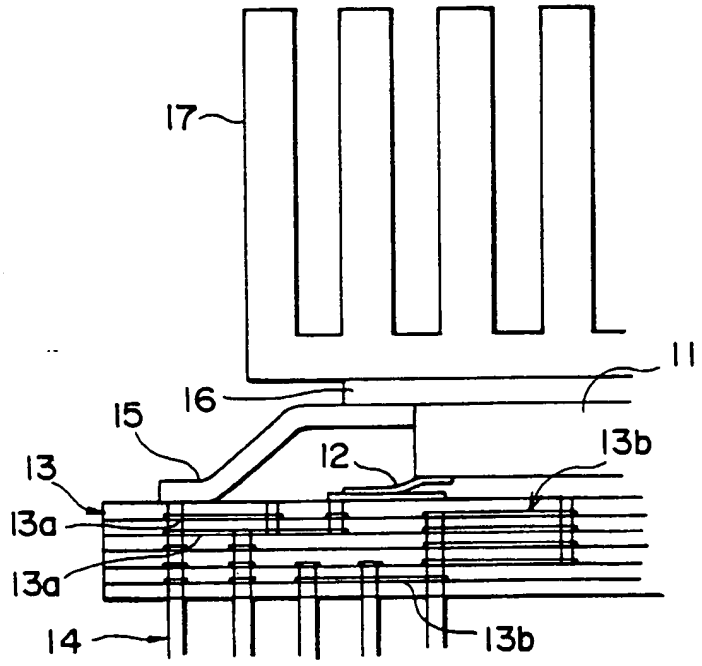

FIG. 2

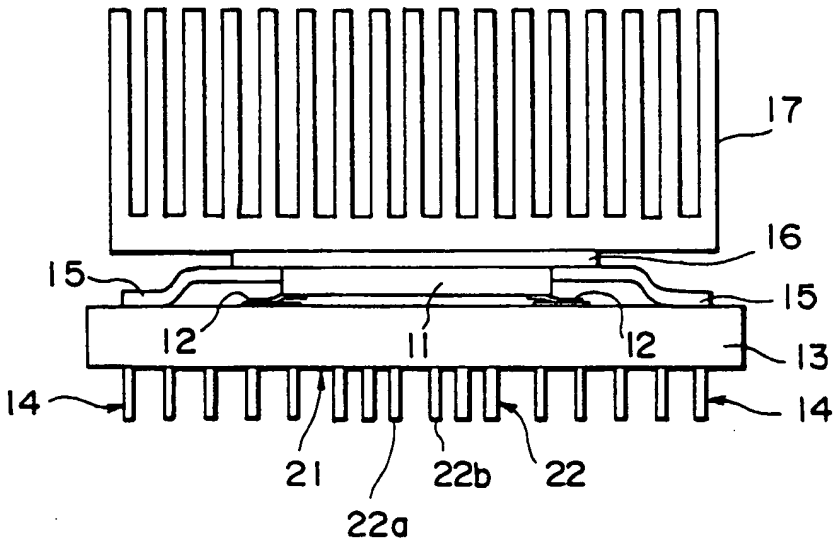

FIG. 3A

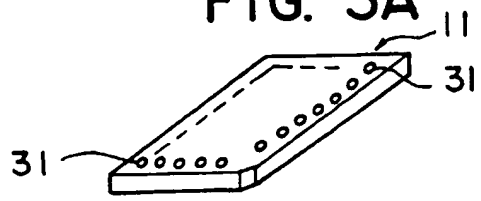

FIG. 3B

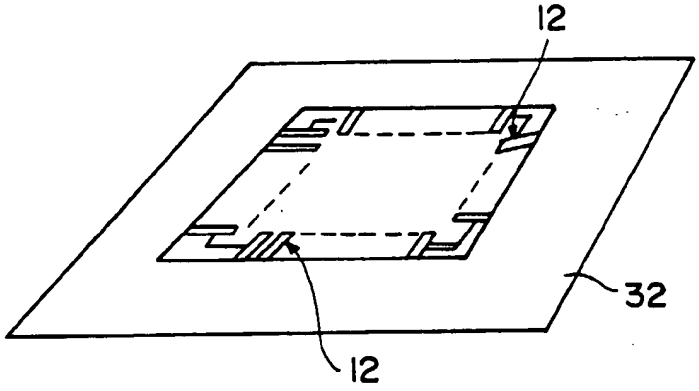

FIG. 3C

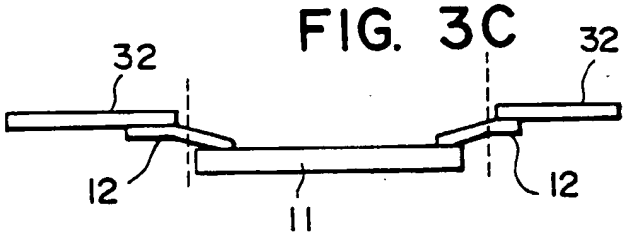

FIG. 3D

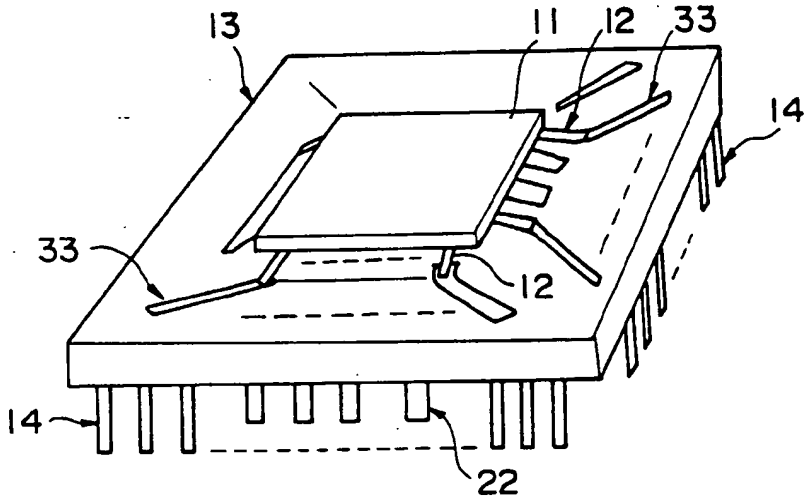

FIG. 3E

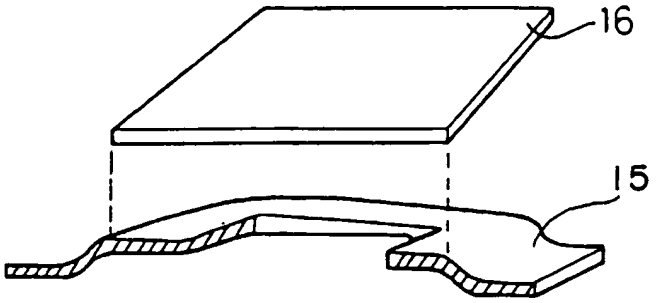

FIG. 3F

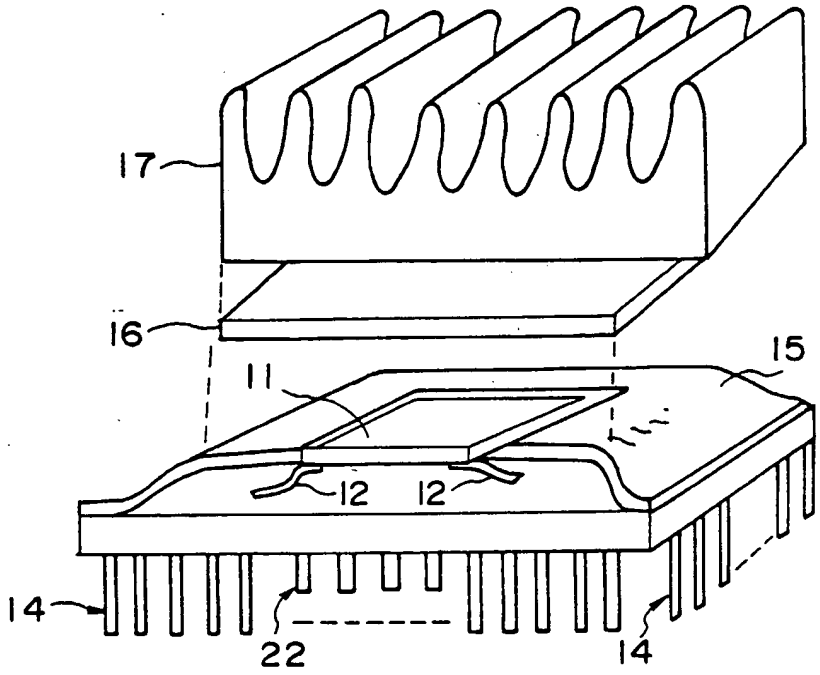

FIG. 4

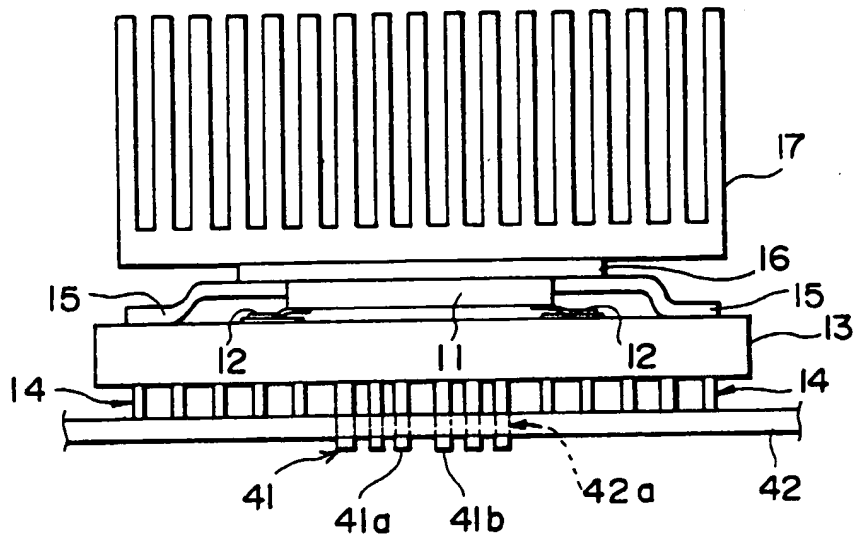
17
16
15
15
13
12
11
12
14
14
41
41a
41b
42a
42

FIG. 5

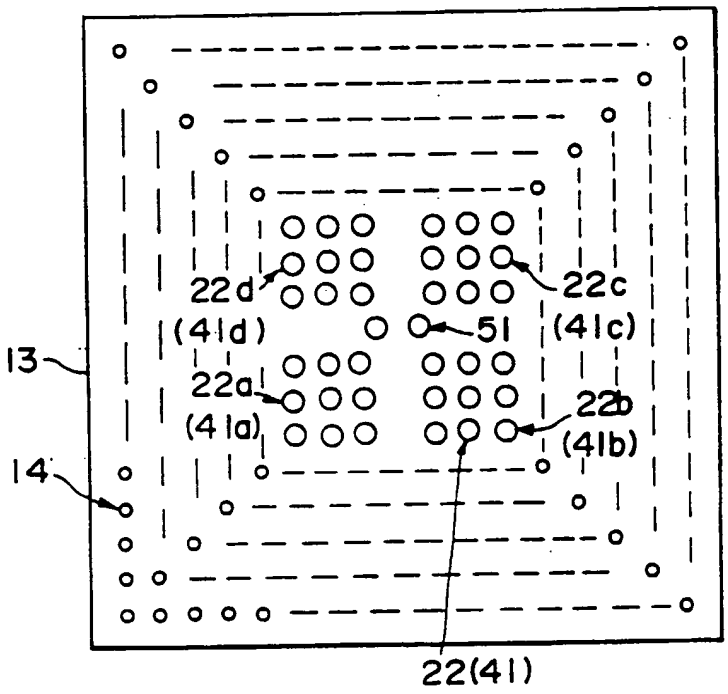
22d
(41d)
22c
(41c)
51
13
22a
(41a)
22b
(41b)
14
22(41)

FIG. 6

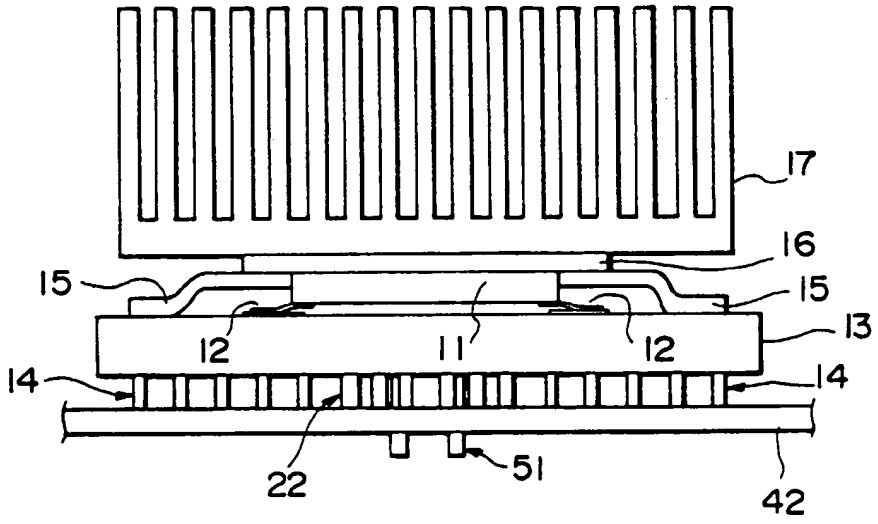

FIG. 7B

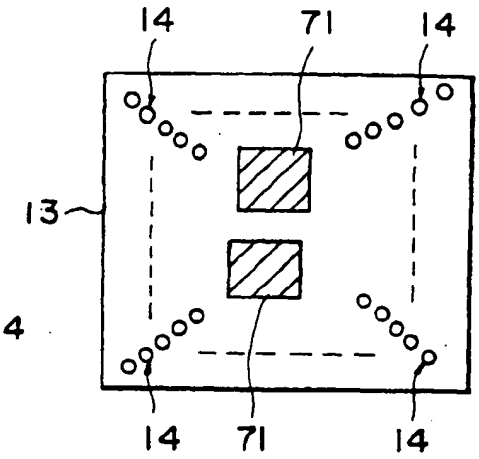

FIG. 7A

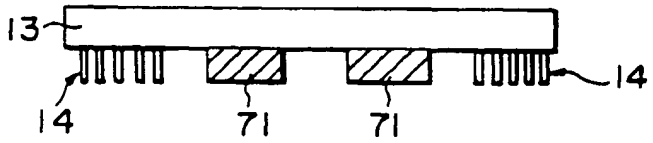

FIG. 8B

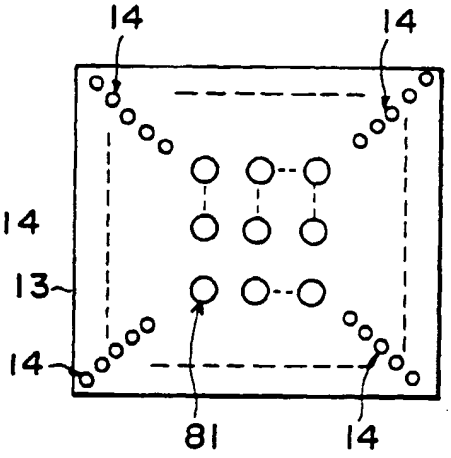

FIG. 8A

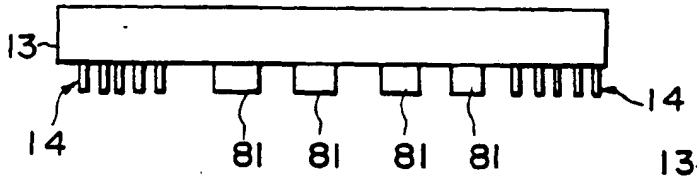

FIG. 9B

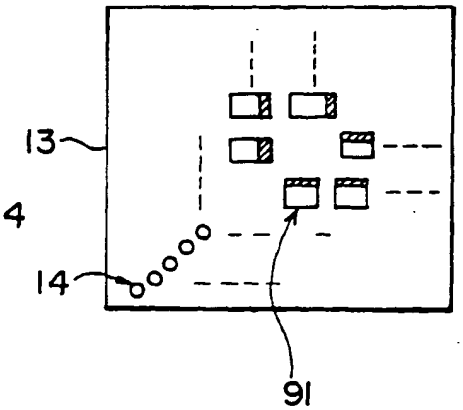

FIG. 9A

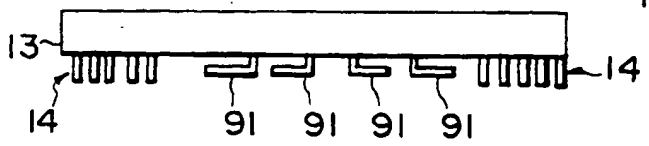

FIG. 10

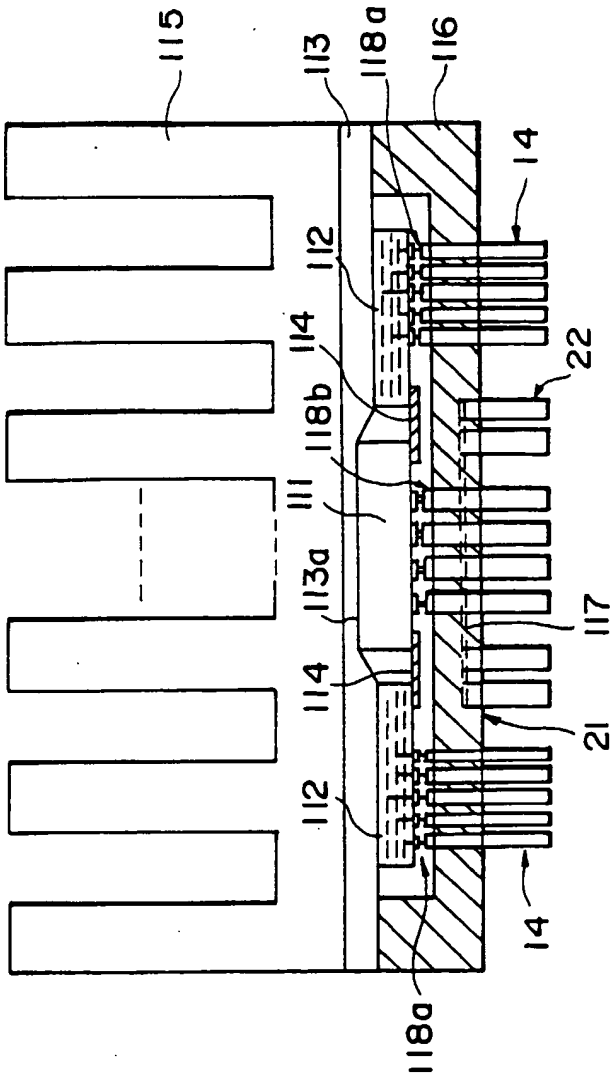
115
113
118a
116
14
112
114
22
118b
111
113a
117
114
21
112
14
118a

FIG. 11A

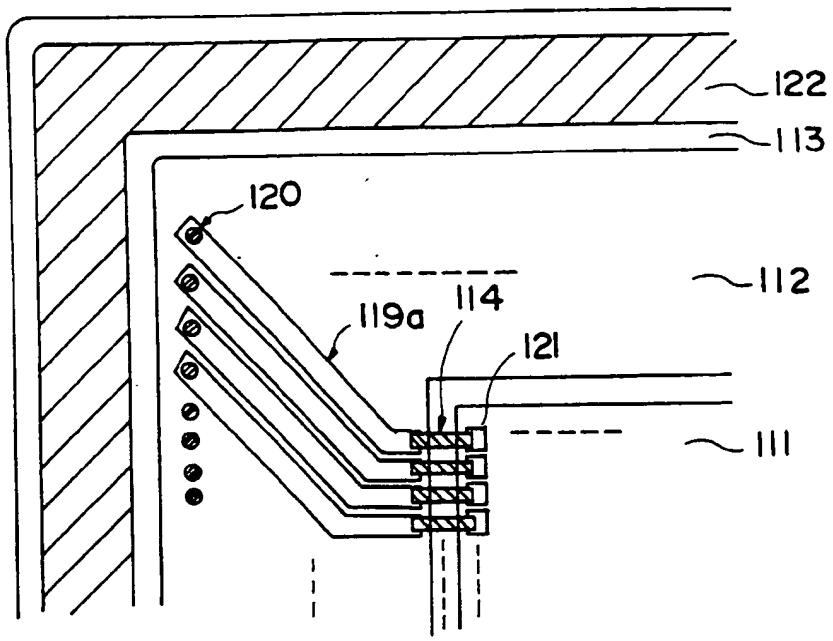

FIG. 11B

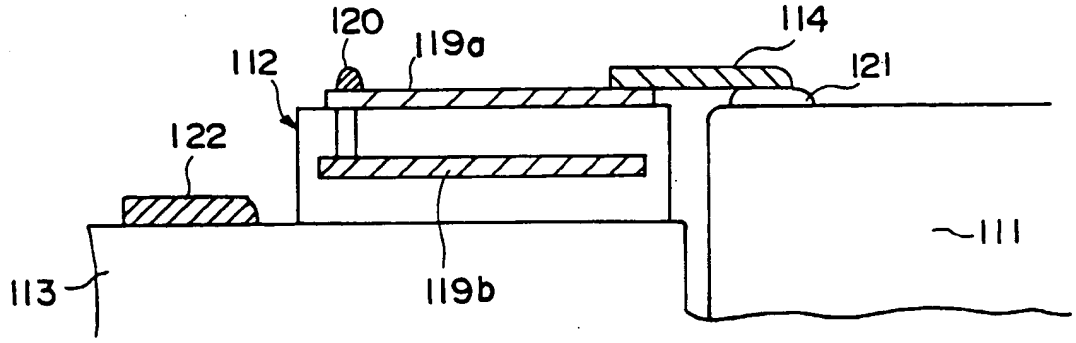

FIG. 11C

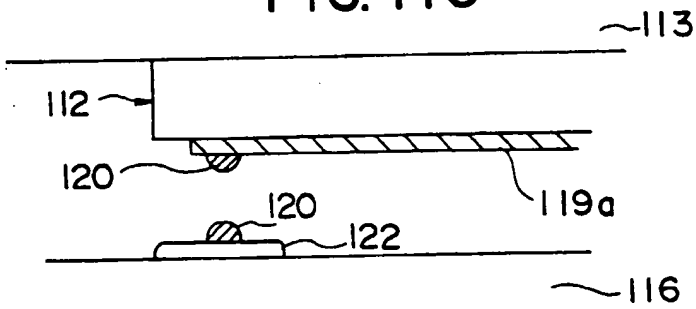

FIG. 12A

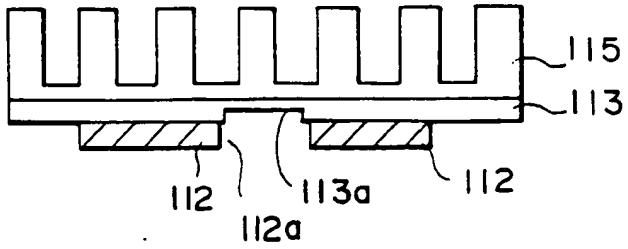

FIG. 12B

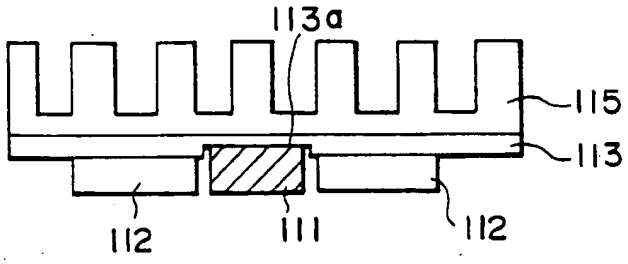

FIG. 12C

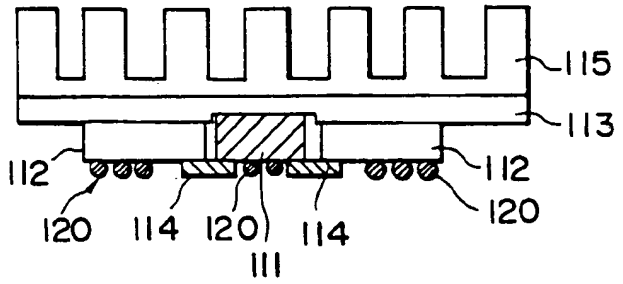

FIG. 12D

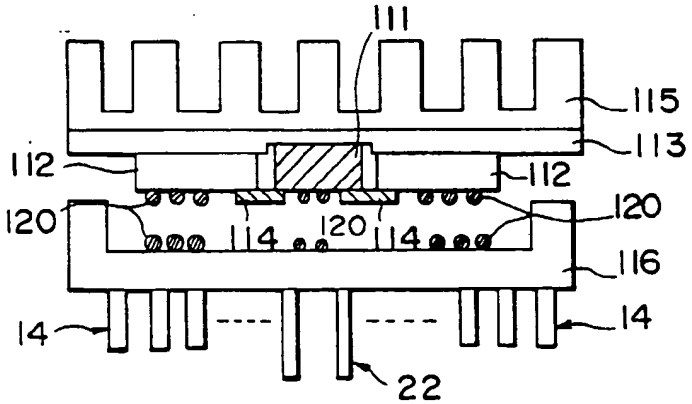

FIG. 13A

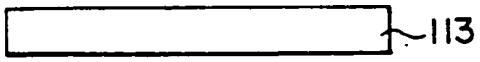

FIG. 13B

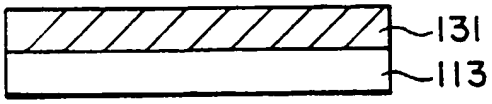

FIG. 13C

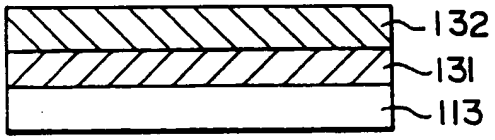

FIG. 13D

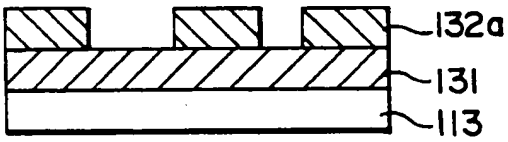

FIG. 13E

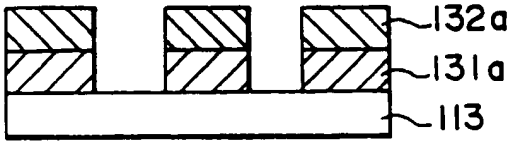

FIG. 13F

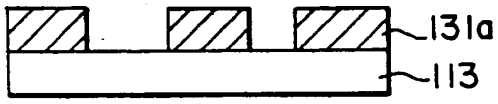

FIG. 13G

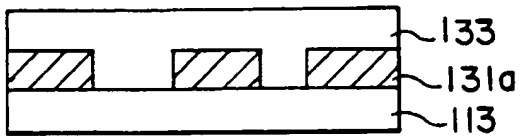

FIG. 13H

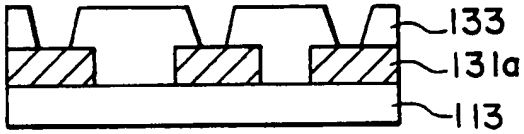

FIG. 13I

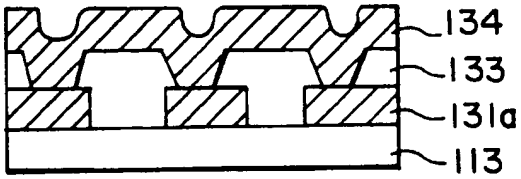

FIG. 14A

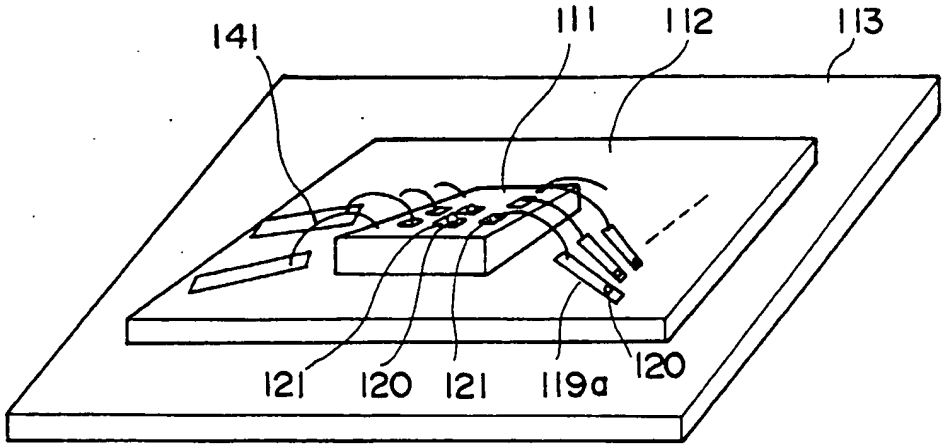

FIG. 14B

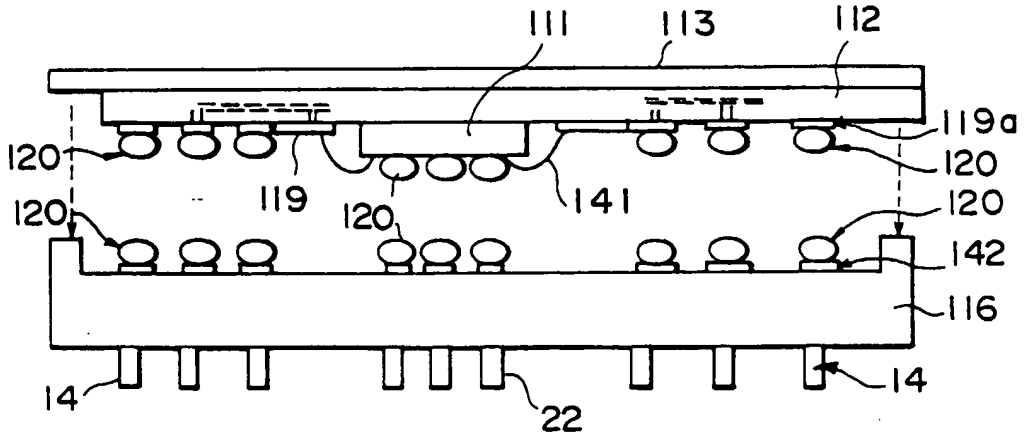

FIG. 15

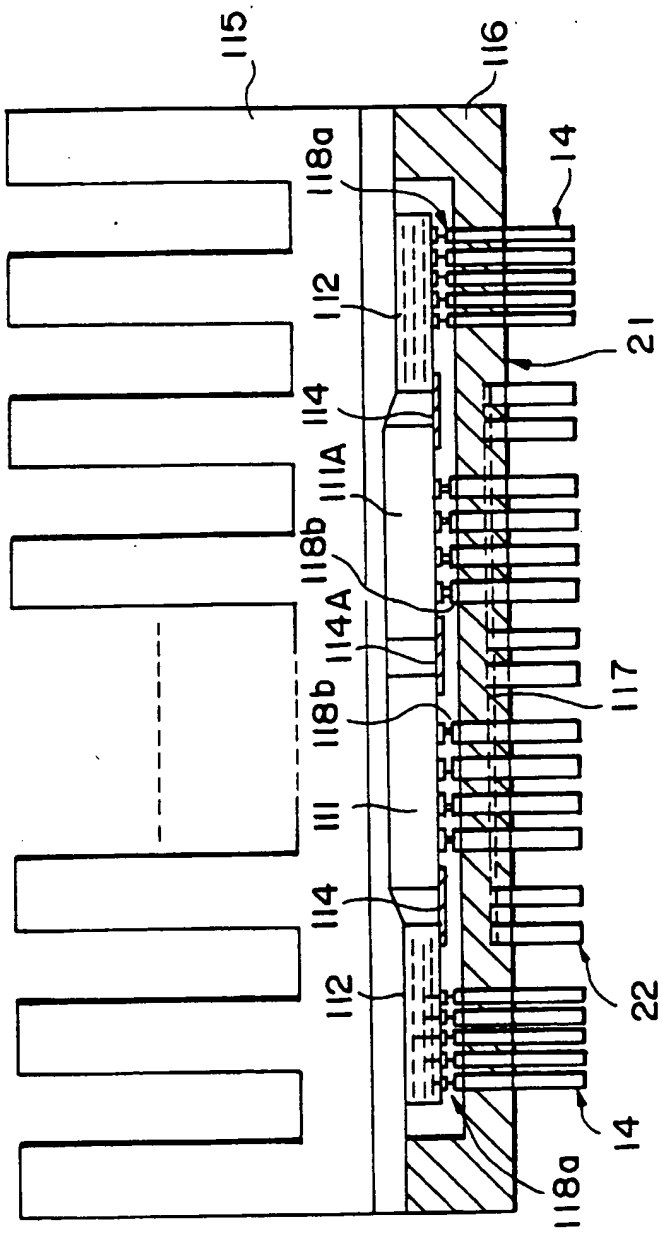
115
116
118a
14
112
21
114
111A
118b
114A
118b
117
111
114
112
22
14
118a

FIG. 16A

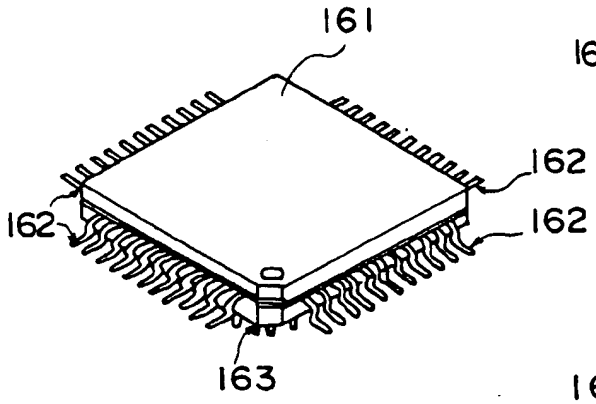

FIG. 16B

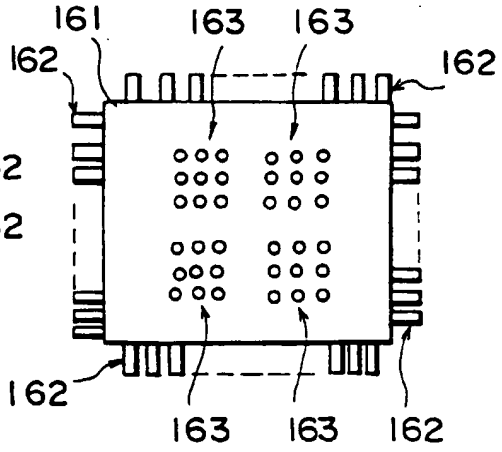

FIG. 17A

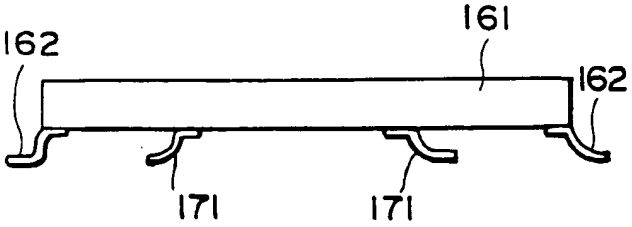

FIG. 17B